

BUL45D2

High Speed, High Gain Bipolar NPN Power Transistor with Integrated Collector-Emitter Diode and Built-in Efficient Antisaturation Network

The BUL45D2 is state-of-art High Speed High gain BiPolar transistor (H2BIP). High dynamic characteristics and lot-to-lot minimum spread (± 150 ns on storage time) make it ideally suitable for light ballast applications. Therefore, there is no need to guarantee an h_{FE} window. It's characteristics make it also suitable for PFC application.

Features

- Low Base Drive Requirement
- High Peak DC Current Gain (55 Typical) @ $I_C = 100$ mA
- Extremely Low Storage Time Min/Max Guarantees Due to the H2BIP Structure which Minimizes the Spread
- Integrated Collector-Emitter Free Wheeling Diode
- Fully Characterized and Guaranteed Dynamic $V_{CE(sat)}$
- "6 Sigma" Process Providing Tight and Reproducible Parameter Spreads
- Pb-Free Package is Available*

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Sustaining Voltage	V_{CEO}	400	Vdc
Collector-Base Breakdown Voltage	V_{CBO}	700	Vdc
Collector-Emitter Breakdown Voltage	V_{CES}	700	Vdc
Emitter-Base Voltage	V_{EBO}	12	Vdc
Collector Current – Continuous	I_C	5	Adc
– Peak (Note 1)	I_{CM}	10	
Base Current – Continuous	I_B	2	Adc
– Peak (Note 1)	I_{BM}	4	
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	75 0.6	W W/ $^\circ\text{C}$
Operating and Storage Temperature	T_J, T_{stg}	-65 to 150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.65	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	$^\circ\text{C/W}$
Maximum Lead Temperature for Soldering Purposes 1/8" from Case for 5 Seconds	T_L	260	$^\circ\text{C}$

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Pulse Test: Pulse Width = 5 ms, Duty Cycle $\leq 10\%$.

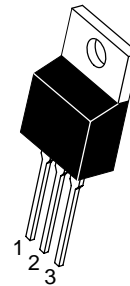
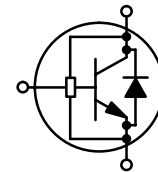
*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



ON Semiconductor®

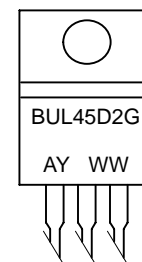
<http://onsemi.com>

**POWER TRANSISTOR
5.0 AMPERES,
700 VOLTS, 75 WATTS**



TO-220AB
CASE 221A-09
STYLE 1

MARKING DIAGRAM



A = Assembly
Location
Y = Year
WW = Work Week
G = Pb-Free Pack-

ORDERING INFORMATION

Device	Package	Shipping
BUL45D2	TO-220	50 Units / Rail
BUL45D2G	TO-220 (Pb-Free)	50 Units / Rail

BUL45D2

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage ($I_C = 100\text{ mA}$, $L = 25\text{ mH}$)	$V_{CEO(sus)}$	400	450		Vdc
Collector–Base Breakdown Voltage ($I_{CBO} = 1\text{ mA}$)	V_{CBO}	700	910		Vdc
Emitter–Base Breakdown Voltage ($I_{EBO} = 1\text{ mA}$)	V_{EBO}	12	14.1		Vdc
Collector Cutoff Current ($V_{CE} = \text{Rated } V_{CEO}$, $I_B = 0$)	I_{CEO}			100	μA dc
Collector Cutoff Current ($V_{CE} = \text{Rated } V_{CES}$, $V_{EB} = 0$) ($V_{CE} = 500\text{ V}$, $V_{EB} = 0$)	@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$ I_{CES}			100 500 100	μA dc
Emitter–Cutoff Current ($V_{EB} = 10\text{ Vdc}$, $I_C = 0$)	I_{EBO}			100	μA dc

ON CHARACTERISTICS

Base–Emitter Saturation Voltage ($I_C = 0.8\text{ Adc}$, $I_B = 80\text{ mAdc}$) ($I_C = 2\text{ Adc}$, $I_B = 0.4\text{ Adc}$)	@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$ @ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$	$V_{BE(sat)}$		0.8 0.7 0.89 0.79	1 0.9 1 0.9	Vdc
Collector–Emitter Saturation Voltage ($I_C = 0.8\text{ Adc}$, $I_B = 80\text{ mAdc}$) ($I_C = 2\text{ Adc}$, $I_B = 0.4\text{ Adc}$) ($I_C = 0.8\text{ Adc}$, $I_B = 40\text{ mAdc}$)	@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$ @ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$ @ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$	$V_{CE(sat)}$		0.28 0.32 0.32 0.38 0.46 0.62	0.4 0.5 0.5 0.6 0.75 1	Vdc
DC Current Gain ($I_C = 0.8\text{ Adc}$, $V_{CE} = 1\text{ Vdc}$) ($I_C = 2\text{ Adc}$, $V_{CE} = 1\text{ Vdc}$)	@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$ @ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$	h_{FE}	22 20 10 7	34 29 14 9.5	—	

DIODE CHARACTERISTICS

Forward Diode Voltage ($I_{EC} = 1\text{ Adc}$) ($I_{EC} = 2\text{ Adc}$) ($I_{EC} = 0.4\text{ Adc}$)	@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$ @ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$ @ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$	V_{EC}		1.04 0.7 1.2 0.85 0.62	1.5 1.6 1.2	V
Forward Recovery Time (see Figure 27) ($I_F = 1\text{ Adc}$, $di/dt = 10\text{ A}/\mu\text{s}$) ($I_F = 2\text{ Adc}$, $di/dt = 10\text{ A}/\mu\text{s}$) ($I_F = 0.4\text{ Adc}$, $di/dt = 10\text{ A}/\mu\text{s}$)	@ $T_C = 25^\circ\text{C}$ @ $T_C = 25^\circ\text{C}$ @ $T_C = 25^\circ\text{C}$	T_{fr}		330 360 320		ns

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ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTICS					
Current Gain Bandwidth (I _C = 0.5 Adc, V _{CE} = 10 Vdc, f = 1 MHz)	f _T		13		MHz
Output Capacitance (V _{CB} = 10 Vdc, I _E = 0, f = 1 MHz)	C _{ob}		50	75	pF
Input Capacitance (V _{EB} = 8 Vdc)	C _{ib}		340	500	pF

DYNAMIC SATURATION VOLTAGE

Dynamic Saturation Voltage: Determined 1 μs and 3 μs respectively after rising I _{B1} reaches 90% of final I _{B1}	I _C = 1 A I _{B1} = 100 mA V _{CC} = 300 V	@ 1 μs	@ T _C = 25°C @ T _C = 125°C	V _{CE(dsat)}		3.7 9.4		V
		@ 3 μs	@ T _C = 25°C @ T _C = 125°C			0.35 2.7		V
	I _C = 2 A I _{B1} = 0.8 A V _{CC} = 300 V	@ 1 μs	@ T _C = 25°C @ T _C = 125°C		3.9 12		V	
		@ 3 μs	@ T _C = 25°C @ T _C = 125°C		0.4 1.5		V	

SWITCHING CHARACTERISTICS: Resistive Load (D.C. ≤ 10%, Pulse Width = 20 μs)

Turn-on Time	I _C = 2 Adc, I _{B1} = 0.4 Adc I _{B2} = 1 Adc V _{CC} = 300 Vdc	@ T _C = 25°C @ T _C = 125°C	t _{on}		90 105	150	ns
Turn-off Time		@ T _C = 25°C @ T _C = 125°C	t _{off}		1.15 1.5	1.3	μs
Turn-on Time	I _C = 2 Adc, I _{B1} = 0.4 Adc I _{B2} = 0.4 Adc V _{CC} = 300 Vdc	@ T _C = 25°C @ T _C = 125°C	t _{on}		90 110	150	ns
Turn-off Time		@ T _C = 25°C @ T _C = 125°C	t _{off}	2.1	3.1	2.4	μs

SWITCHING CHARACTERISTICS: Inductive Load (V_{clamp} = 300 V, V_{CC} = 15 V, L = 200 μH)

Fall Time	I _C = 1 Adc I _{B1} = 100 mAAdc I _{B2} = 500 mAAdc	@ T _C = 25°C @ T _C = 125°C	t _f		90 93	150	ns
Storage Time		@ T _C = 25°C @ T _C = 125°C	t _s		0.72 1.05	0.9	μs
Crossover Time		@ T _C = 25°C @ T _C = 125°C	t _c		95 95	150	ns
Fall Time	I _C = 2 Adc I _{B1} = 0.4 Adc I _{B2} = 0.4 Adc	@ T _C = 25°C @ T _C = 125°C	t _f		80 105	150	ns
Storage Time		@ T _C = 25°C @ T _C = 125°C	t _s	1.95	2.9	2.25	μs
Crossover Time		@ T _C = 25°C @ T _C = 125°C	t _c		225 450	300	ns

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TYPICAL STATIC CHARACTERISTICS

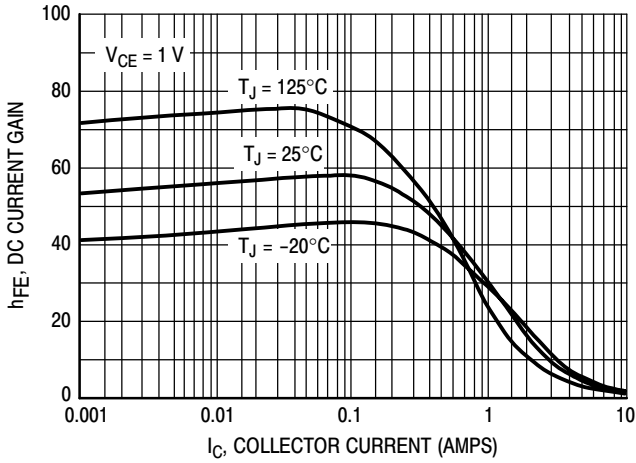


Figure 1. DC Current Gain @ 1 Volt

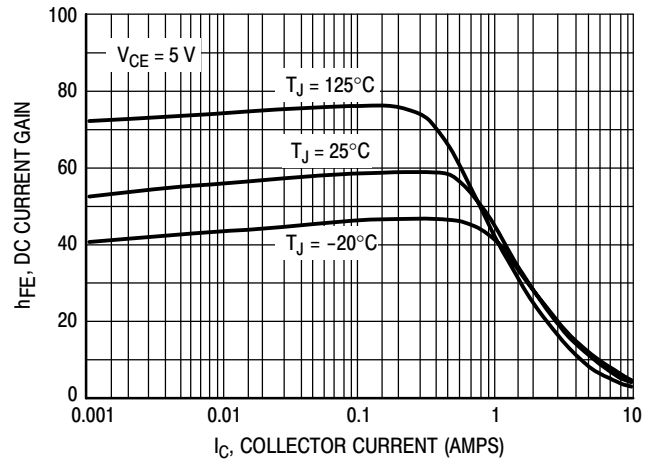


Figure 2. DC Current Gain @ 5 Volt

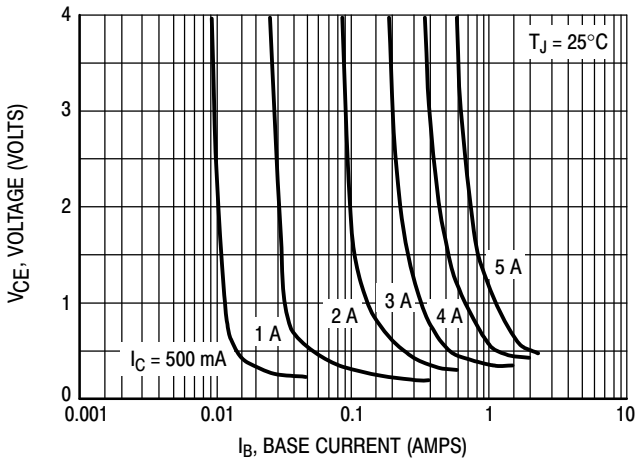


Figure 3. Collector Saturation Region

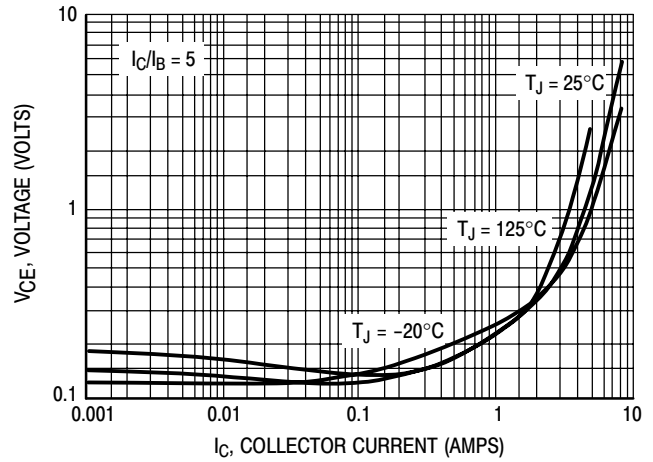


Figure 4. Collector-Emitter Saturation Voltage

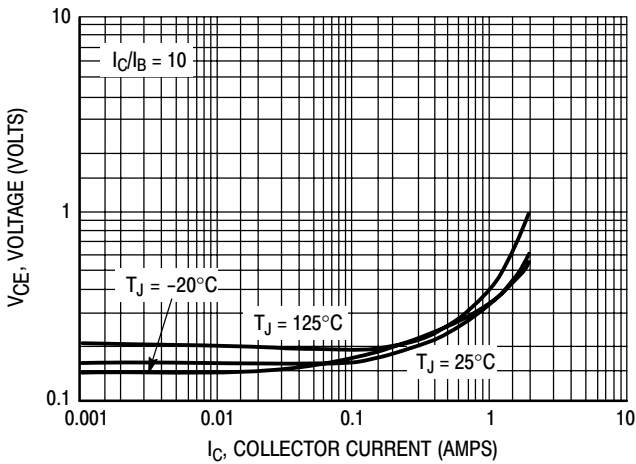


Figure 5. Collector-Emitter Saturation Voltage

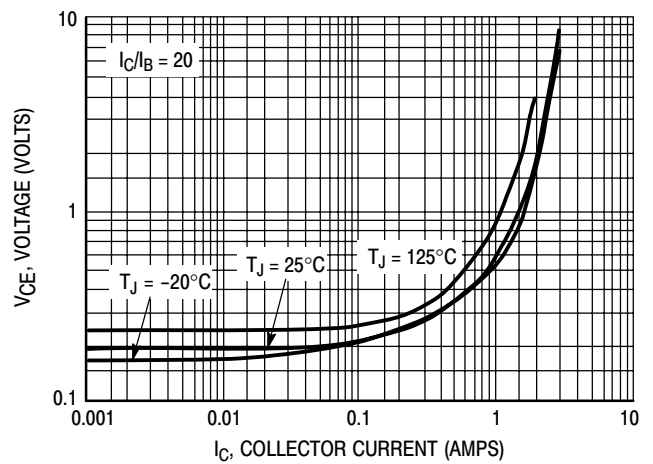


Figure 6. Collector-Emitter Saturation Voltage

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TYPICAL STATIC CHARACTERISTICS

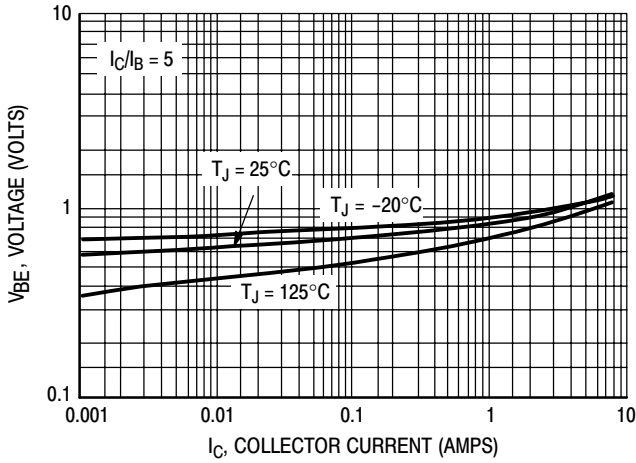


Figure 7. Base-Emitter Saturation Region

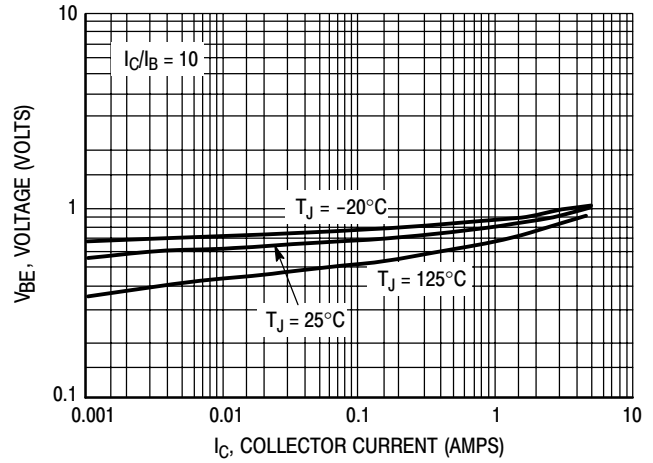


Figure 8. Base-Emitter Saturation Region

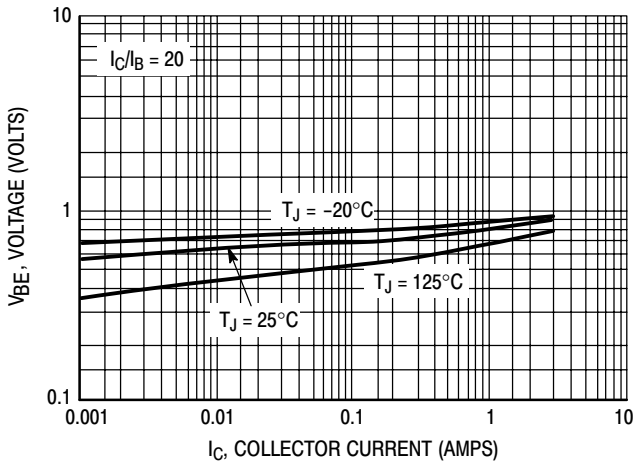


Figure 9. Base-Emitter Saturation Region

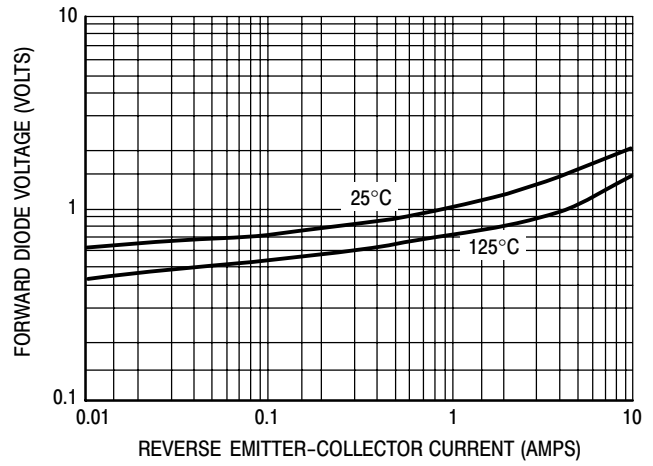


Figure 10. Forward Diode Voltage

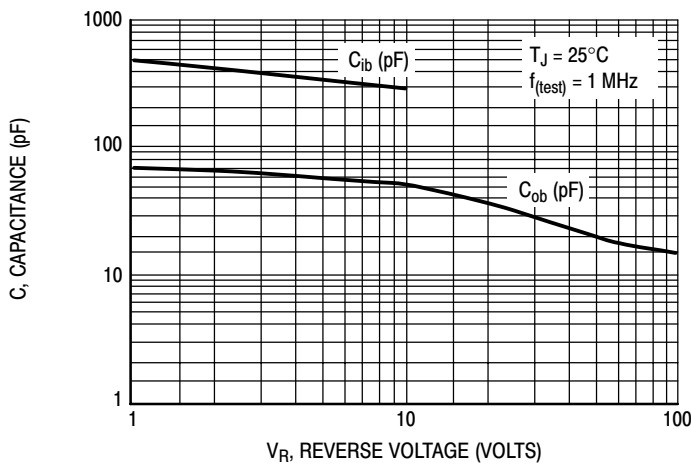


Figure 11. Capacitance

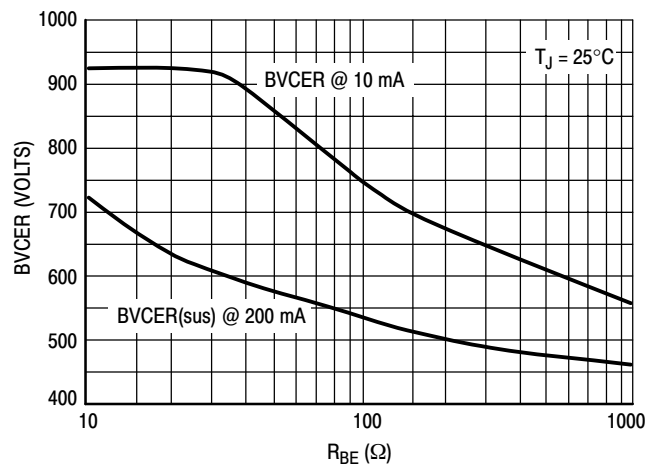


Figure 12. BVCEr = f(ICER)

TYPICAL SWITCHING CHARACTERISTICS

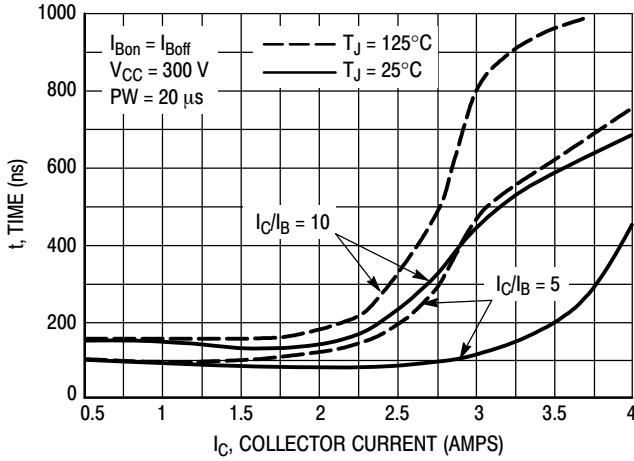


Figure 13. Resistive Switch Time, t_{on}

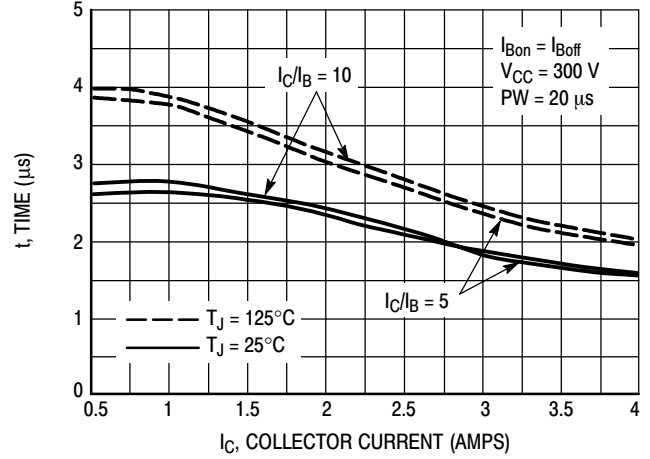


Figure 14. Resistive Switch Time, t_{off}

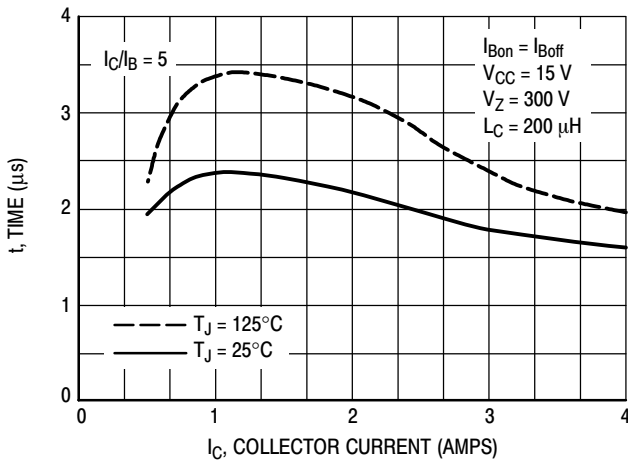


Figure 15. Inductive Storage Time, t_{si} @ $I_C/I_B = 5$

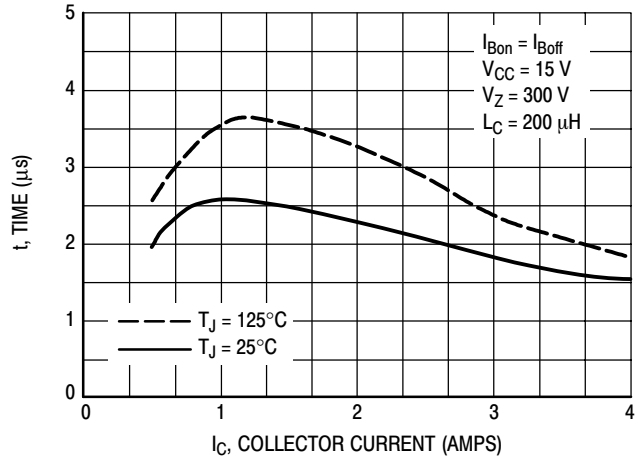


Figure 16. Inductive Storage Time, t_{si} @ $I_C/I_B = 10$

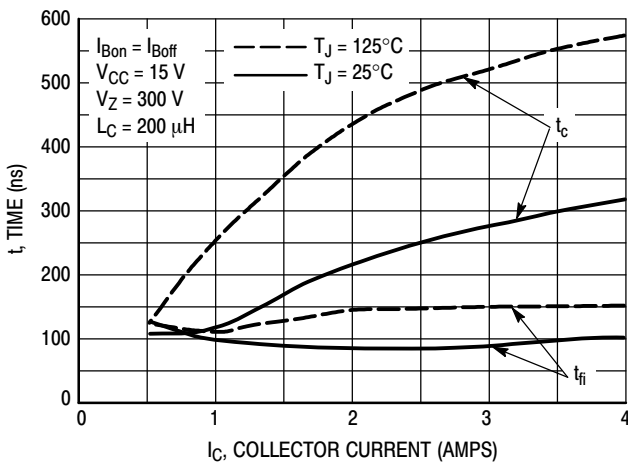


Figure 17. Inductive Switching, t_c & t_{fi} @ $I_C/I_B = 5$

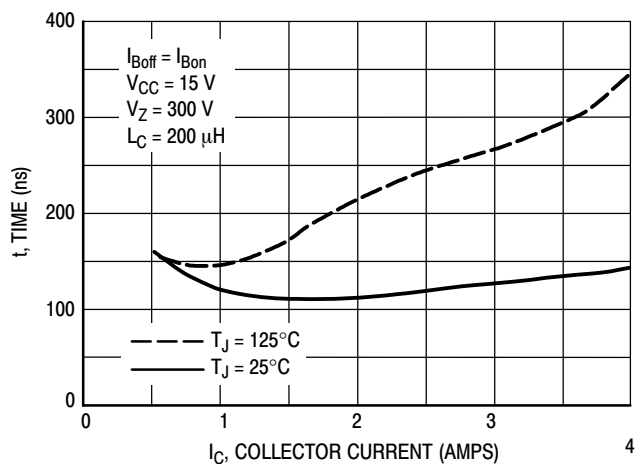


Figure 18. Inductive Switching, t_{fi} @ $I_C/I_B = 10$

TYPICAL SWITCHING CHARACTERISTICS

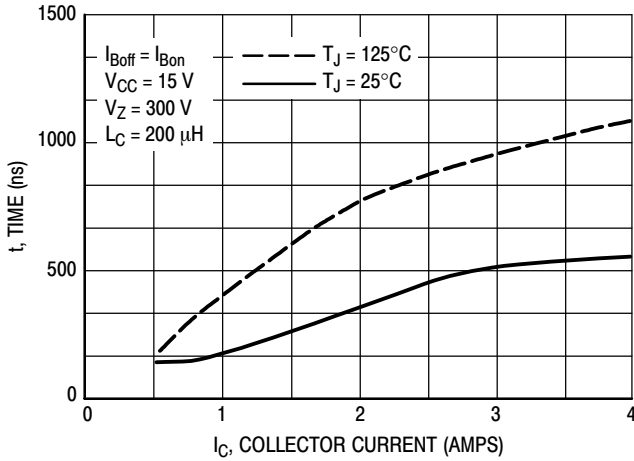


Figure 19. Inductive Switching, t_t @ $I_C/I_B = 10$

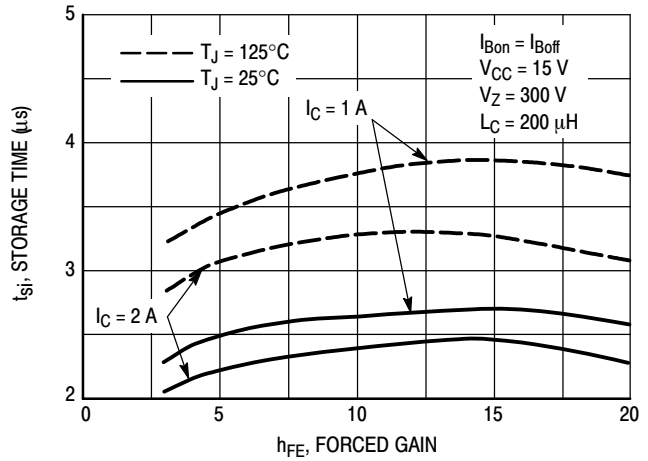


Figure 20. Inductive Storage Time

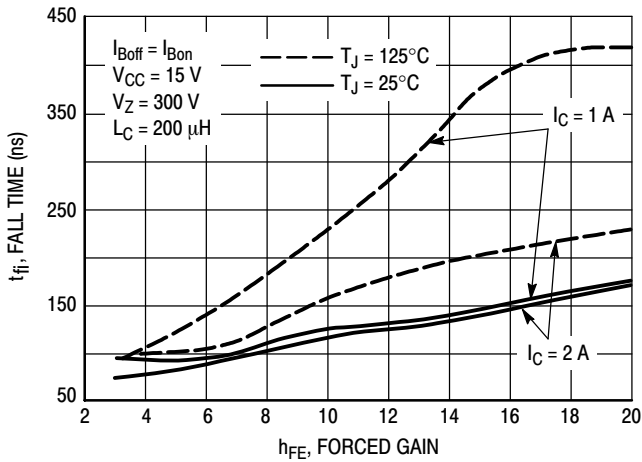


Figure 21. Inductive Fall Time

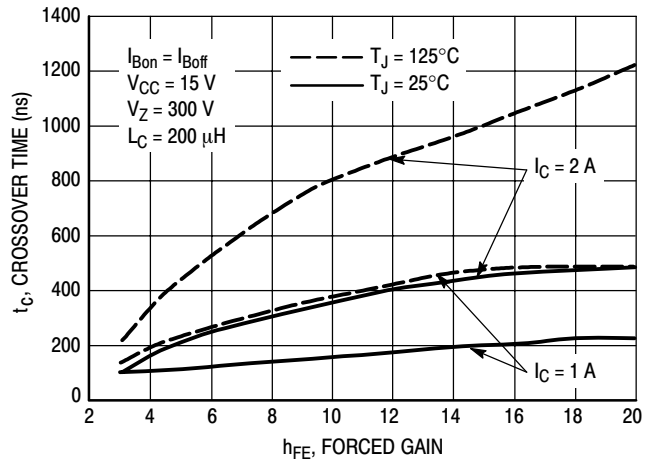


Figure 22. Inductive Crossover Time

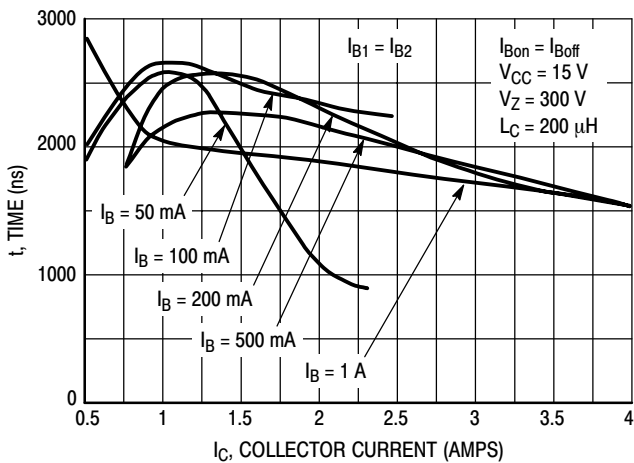


Figure 23. Inductive Storage Time, t_{si}

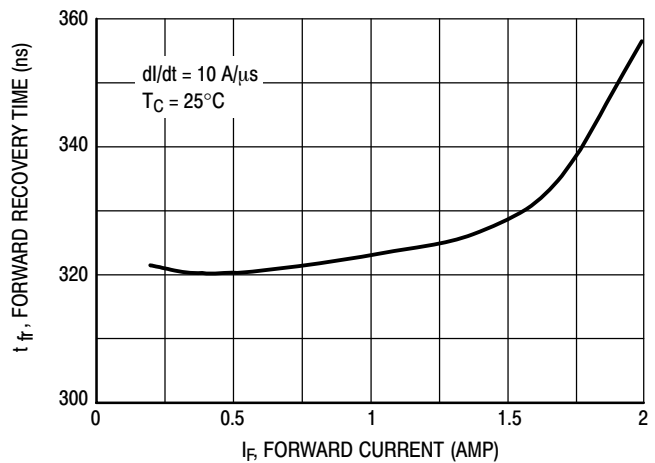


Figure 24. Forward Recovery Time t_{fr}

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TYPICAL SWITCHING CHARACTERISTICS

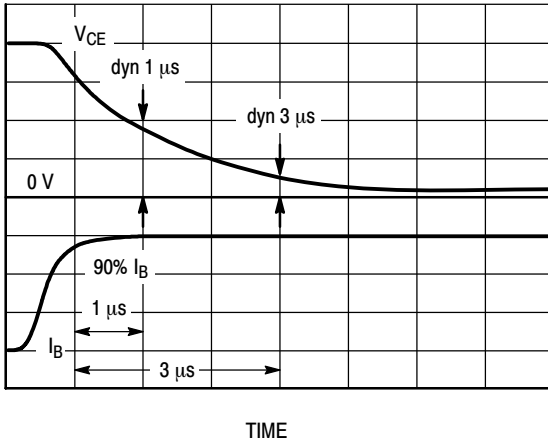


Figure 25. Dynamic Saturation Voltage Measurements

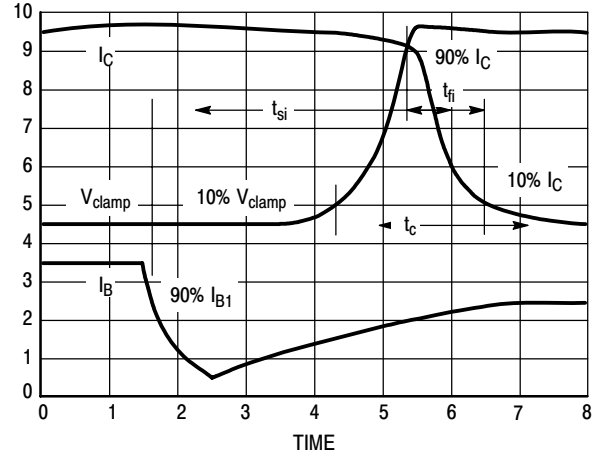


Figure 26. Inductive Switching Measurements

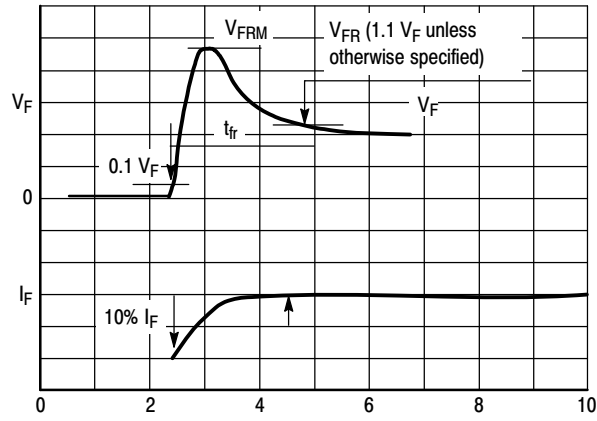
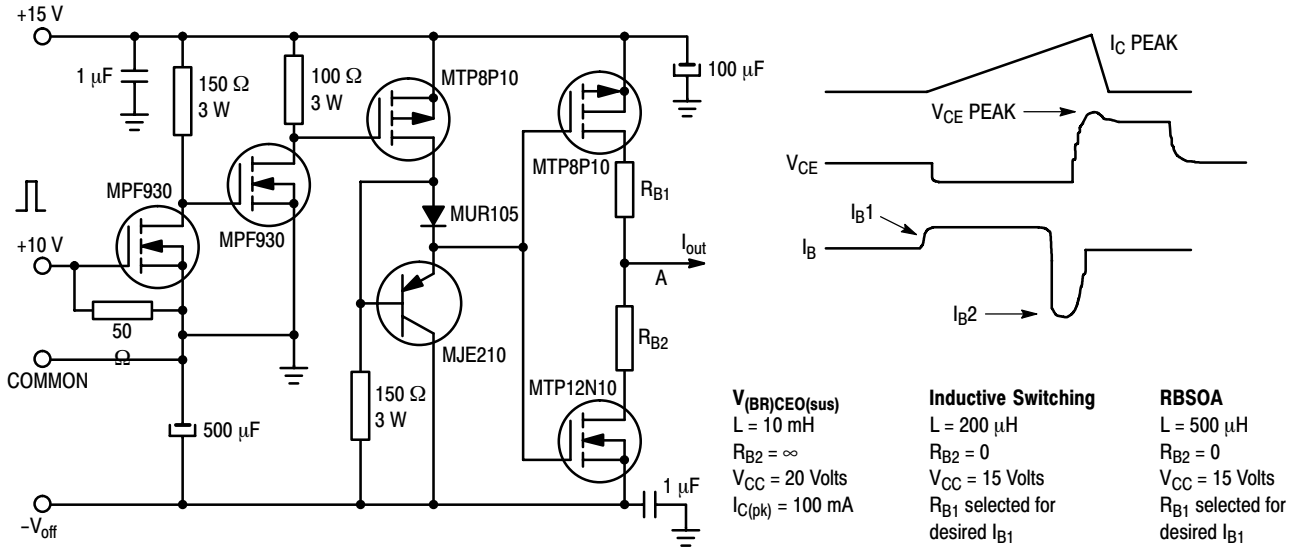


Figure 27. t_{fr} Measurements

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TYPICAL SWITCHING CHARACTERISTICS

Table 1. Inductive Load Switching Drive Circuit



TYPICAL CHARACTERISTICS

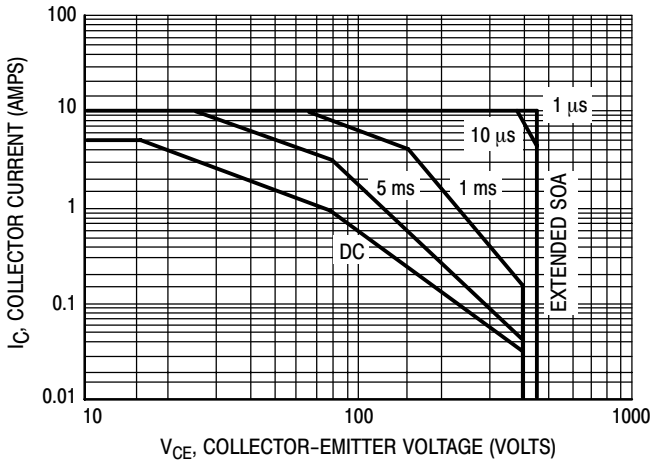


Figure 28. Forward Bias Safe Operating Area

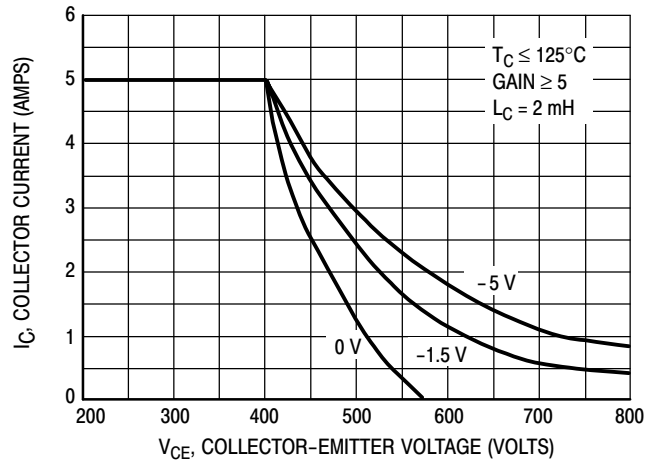


Figure 29. Reverse Bias Safe Operating Area

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TYPICAL CHARACTERISTICS

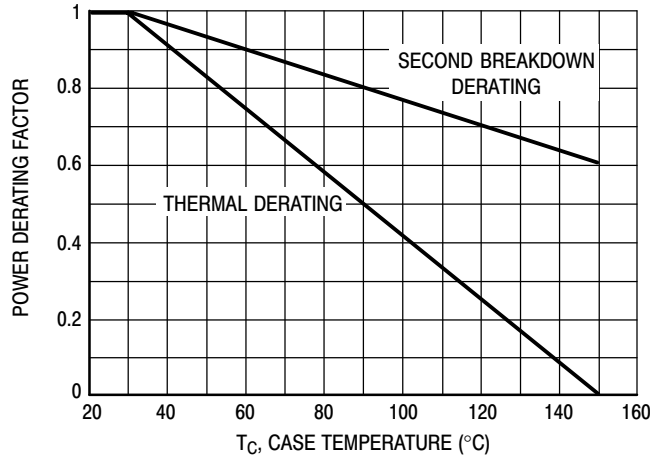


Figure 30. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 28 is based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C > 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on

Figure 28 may be found at any case temperature by using the appropriate curve on Figure 30.

$T_{J(pk)}$ may be calculated from the data in Figure 31. At any case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn-off with the base to emitter junction reverse biased. The safe level is specified as a reverse biased safe operating area (Figure 29). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

TYPICAL THERMAL RESPONSE

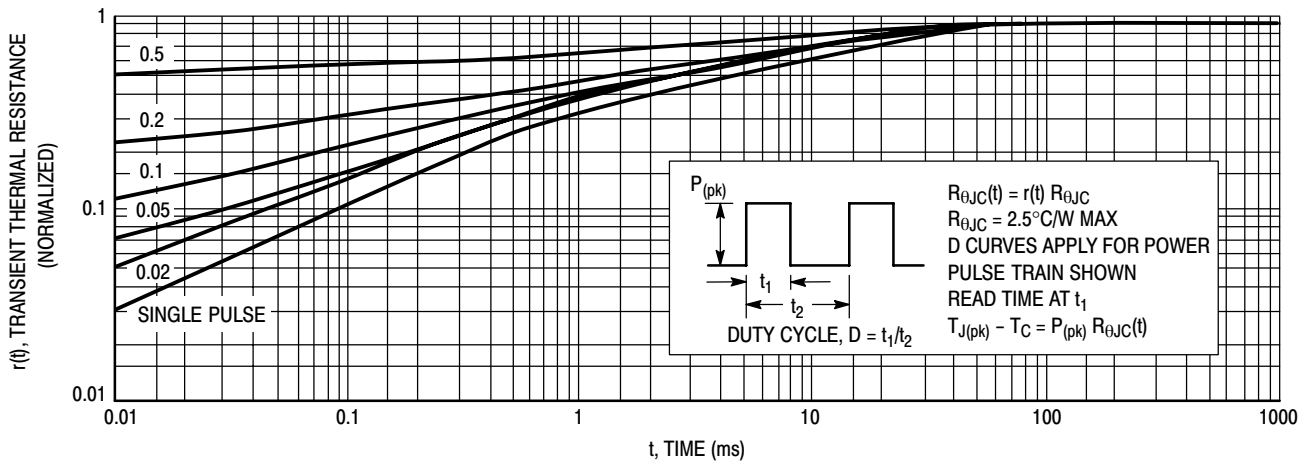
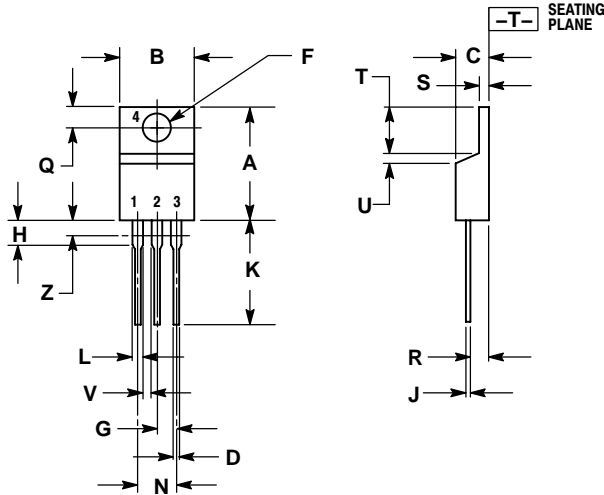


Figure 31. Typical Thermal Response ($Z_{\theta JC}(t)$) for BUL45D2

BUL45D2

PACKAGE DIMENSIONS

TO-220AB
CASE 221A-09
ISSUE AA



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

STYLE 1:

- PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

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